September 2006 Advance Information



Vcc

GND

AS7C513C

Features

- Industrial (-40° to 85°C) temperature
- Organization: 32,768 words \times 16 bits
- Center power and ground pins for low noise
- High speed
- 12 ns address access time
- 6 ns output enable access time
- Low power consumption via chip deselect
- Easy memory expansion with \overline{CE} , \overline{OE} inputs
- TTL-compatible, three-state I/O
- Upper and Lower byte pin

- JEDEC standard packaging
- 44-pin 400 mil SOJ
- 44-pin TSOP 2
- ESD protection ≥ 2000 volts

Pin arrangement

44-Pin SOJ (400 mil), TSOP 2

Logic block diagram A0 decoder A1 A2 32,768 x 16 A3 Array Address A4 A5 A6 A7 I/O0–I/O7 I/O8–I/O15 I/O buffer Control circuit WE -Address decoder A9 A9 A12 A13 A14 A10 A11 UB

12/5/06, v 1.0

OE LB CE

Functional description

The AS7C513C is a 5V high-performance CMOS 524,288-bit Static Random Access Memory (SRAM) device organized as 32,768 words $\times 16$ bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 12 ns with output enable access times (t_{OE}) of 6 ns are ideal for high-performance applications.

When \overline{CE} is high, the device enters standby mode. If inputs are still toggling, the device will consume I_{SB} power. If the bus is static, then full standby power is reached (I_{SB1}).

A write cycle is accomplished by asserting write enable (\overline{WE}) and chip enable (\overline{CE}). Data on the input pins I/O0 through I/O15 is written on the rising edge of \overline{WE} (write cycle 1) or \overline{CE} (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable (\overline{OE}) or write enable (\overline{WE}).

A read cycle is accomplished by asserting output enable (\overline{OE}) and chip enable (\overline{CE}) with write enable (\overline{WE}) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive or write enable is active, output drivers stay in high-impedance mode.

The device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{\text{LB}}$ controls the lower bits, I/O0 through I/O7, and $\overline{\text{UB}}$ controls the higher bits, I/O8 through I/O15.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5 V supply. The AS7C513C is packaged in common industry standard packages.

Parameter	Symbol	Min	Max	Unit
Voltage on V _{CC} relative to GND	V _{t1}	-0.50	+7.0	V
Voltage on any pin relative to GND	V _{t2}	-0.50	V _{CC} +0.50	V
Power dissipation	P _D	-	1.25	W
Storage temperature (plastic)	T _{stg}	-55	+125	°C
Ambient temperature with VCC applied	T _{bias}	-55	+125	°C
DC current into outputs (low)	I _{OUT}	-	50	mA

Absolute maximum ratings

Note:

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

CE	WE	OE	LB	UB	I/O0–I/O7	I/O8–I/O15	Mode
Н	Х	Х	Х	Х	High Z	High Z	Standby (I _{SB}), I _{SBI})
L	Н	L	L	Н	D _{OUT}	High Z	Read I/O0–I/O7 (I _{CC})
L	Н	L	Н	L	High Z	D _{OUT}	Read I/O8–I/O15 (I _{CC)}
L	Н	L	L	L	D _{OUT}	D _{OUT}	Read I/O0–I/O15 (I _{CC})
L	L	Х	L	L	D _{IN}	D _{IN}	Write I/O0–I/O15 (I _{CC})
L	L	Х	L	Н	D _{IN}	High Z	Write I/O0–I/O7 (I _{CC})
L	L	Х	Н	L	High Z	D _{IN}	Write I/O8–I/O15 (I _{CC})
L L	H X	H X	X H	X H	High Z	High Z	Output disable (I _{CC})

Key: H = high, L = low, X = don't care.

12/5/06, v 1.0



Recommended operating conditions

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input voltage	V _{IH}	2.2	_	V _{CC} + 0.5	V
input voltage	V _{IL}	-0.5	-	0.8	V
Ambient operating temperature (Industrial)	T _A	-40	-	85	° C

Notes:

 V_{IL} min = -1.5V for pulse width less than 5ns, once per cycle.

 V_{IH} max = V_{CC} +2.0V for pulse width less than 5ns, once per cycle.

DC operating characteristics (over the operating range) I

			AS7C5	13C-12	
Parameter	Sym	Test conditions	Min	Max	Unit
Input leakage current	I _{LI}	$V_{CC} = Max,$ $V_{IN} = GND$ to V_{CC}	-	5	μA
Output leakage current	I _{LO}	$V_{CC} = Max, \overline{CE} = V_{IH},$ $V_{OUT} = GND \text{ to } V_{CC}$	-	5	μA
Operating power supply current	I _{CC}	$\label{eq:V_CC} \begin{split} & V_{CC} = Max, \\ & \overline{CE} \leq V_{IL}, \ I_{OUT} = 0mA, \\ & f = f_{Max} \end{split}$	_	210	mA
	I _{SB}	$V_{CC} = Max,$ $\overline{CE} \ge V_{IH}, f = f_{Max}$	_	60	mA
Standby power supply current	I _{SB1}	$\begin{split} V_{CC} &= Max, \overline{CE} \geq V_{CC} - 0.2 \text{ V}, \\ V_{IN} \leq 0.2 \text{ V or} \\ V_{IN} \geq V_{CC} - 0.2 \text{ V}, \text{ f} = 0 \end{split}$	_	10	mA
Output voltage	V _{OL}	$I_{OL} = 8 \text{ mA}, V_{CC} = Min$	-	0.4	V
output voltage	V _{OH}	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	2.4	-	V

Capacitance (f = 1MHz, $T_a = 25 \text{ °C}$, $V_{CC} = \text{NOMINAL})^2$

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C _{IN}	A, CE, WE, OE, LB, UB	$V_{IN} = 3dV$	6	pF
I/O capacitance	C _{I/O}	I/O	$V_{OUT} = 3dV$	7	pF

Note:

This parameter is guaranteed by device characterization, but is not production tested.



Read cycle (over the operating range)^{3,9}

		AS7C5	13C-12		
Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	t _{RC}	12	_	ns	
Address access time	t _{AA}	_	12	ns	3
Chip enable (\overline{CE}) access time	t _{ACE}	_	12	ns	3
Output enable (\overline{OE}) access time	t _{OE}	_	7	ns	
Output hold from address change	t _{OH}	4	_	ns	5
CE low to output in low Z	t _{CLZ}	4	_	ns	4, 5
$\overline{\text{CE}}$ high to output in high Z	t _{CHZ}	-	6	ns	4, 5
OE low to output in low Z	t _{OLZ}	0	_	ns	4, 5
Byte select access time	t _{BA}	_	7	ns	
Byte select Low to low Z	t _{BLZ}	0	_	ns	4, 5
Byte select High to high Z	t _{BHZ}	-	6	ns	4, 5
OE high to output in high Z	t _{OHZ}	-	6	ns	4, 5
Power up time	t _{PU}	0	-	ns	4, 5
Power down time	t _{PD}	_	12	ns	4, 5

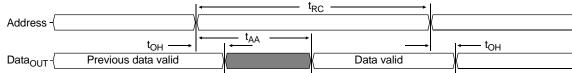
Key to switching waveforms

Rising input

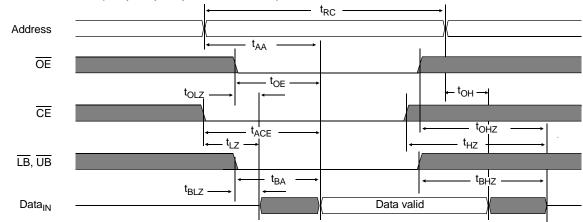
— Falling input

Undefined output/don't care

Read waveform 1 (address controlled)^{3,6,7,9}



Read waveform 2 (OE, CE, UB, LB controlled)^{3,6,8,9}

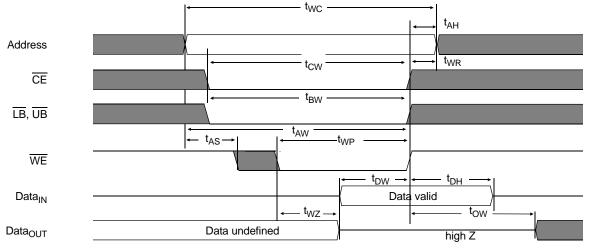




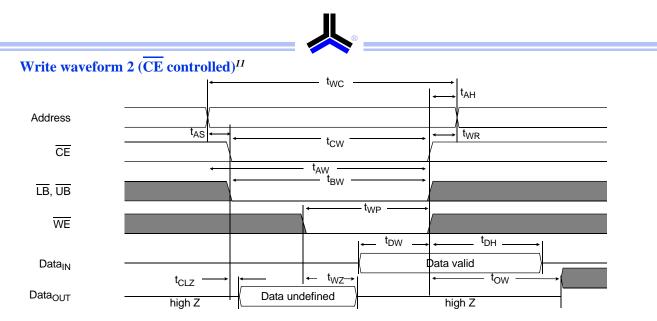
Write cycle (over the operating range) ¹¹

		AS7C513C-12			
Parameter	Symbol	Min	Max	Unit	Notes
Write cycle time	t _{WC}	12	-	ns	
Chip enable (\overline{CE}) to write end	t _{CW}	9	-	ns	
Address setup to write end	t _{AW}	9	-	ns	
Address setup time	t _{AS}	0	-	ns	
Write pulse width	t _{WP}	9	-	ns	
Write recovery time	t _{WR}	0	-	ns	
Address hold from end of write	t _{AH}	0	-	ns	
Data valid to write end	t _{DW}	7	-	ns	
Data hold time	t _{DH}	0	-	ns	5
Write enable to output in high Z	t _{WZ}	_	6	ns	4, 5
Output active from write end	t _{OW}	1	_	ns	4, 5
Byte select low to end of write	t _{BW}	9	—	ns	

Write waveform 1 ($\overline{\text{WE}}$ controlled)¹¹

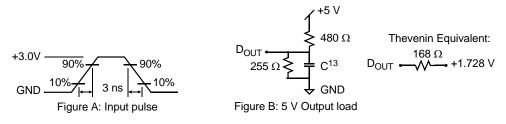


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AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.0 V. See Figure A.
- Input rise and fall times: 3 ns. See Figure A.
- Input and output timing reference levels: 1.5

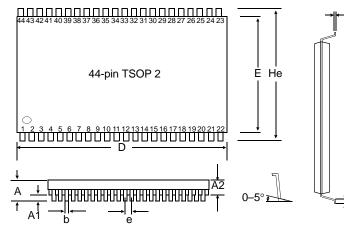


Notes:

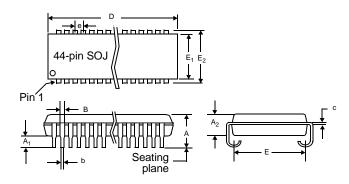
- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CE} is required to meet I_{SB} specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see AC Test Conditions, Figures A and B.
- 4 These parameters are specified with C_L = 5 pF, as in Figures B. Transition is measured \pm 200 mV from steady-state voltage.
- 5 This parameter is guaranteed, but not tested.
- $\overline{\text{WE}}$ is high for read cycle.
- 7 $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low for read cycle.
- 8 Address is valid prior to or coincident with $\overline{\text{CE}}$ transition low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 N/A.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 Not applicable.
- 13 C = 30 pF, except all high Z and low Z parameters where C = 5 pF.



Package dimensions



	44-pin	44-pin TSOP 2			
	Min (mm)	Max (mm)			
Α		1.2			
A1	0.05	0.15			
A2	0.95	1.05			
b	0.30	0.45			
С	0.120	0.21			
D	18.31	18.52			
E	10.06	10.26			
He	11.68	11.94			
е	0.80 (typical)				
l	0.40	0.60			



	44-pin SOJ 400 mil				
	Min (in)	Max (in)			
Α	0.128	0.148			
A ₁	0.025	-			
A ₂	0.105	0.115			
B	0.026	0.032			
b	0.015	0.020			
С	0.007	0.013			
D	1.120	1.130			
E	0.370	NOM			
E ₁	0.395	0.405			
E ₂	0.435	0.445			
e	0.050	NOM			

AS7C513C

Ordering codes

Package	Volt/Temp	12 ns
Plastic SOJ, 400 mil	5V Industrial	AS7C513C-12JIN
TSOP 2, 10.2 x 18.4 mm	5V Industrial	AS7C513C-12TIN

Part numbering system

AS7C	513C	-XX	X	X	X
SRAM prefix	Device number	Access time	Package: J = SOJ 400 mil T = TSOP 2, 10.2 x 18.4 mm	Temperature range: I = industrial: -40° C to 85° C	N = LEAD FREE PART

AS7C1026C



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